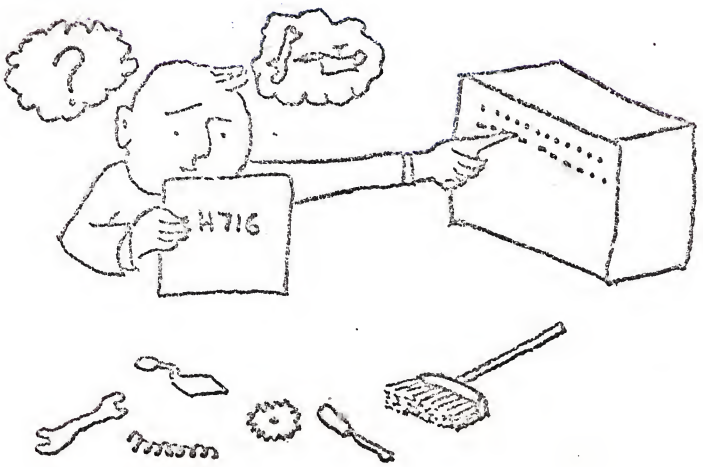
Honeywell H-716

As far as I am aware no handbook was ever produced by the company.

In the UK I built up the attached book which I hope will be of interest to those needing information on the machine.

ROGER BROWN.



FURTHER COPIES FROM ROGER BROWN

BASIC FACTS

Memory Cycle Time	780 775ns ± 20 25ns
Memory Size	4 - 64K
Instruction Complement	78
Circuitry	TTL @ 5 volts
Maximum I/O Transfer Rate	1.2M words/second

PAC LAYOUT

1 - 11	Central Processor
12	ASR or DMC I/O Adaptor
13	Control Panel Connector (With memory module, not controller
14	Memory Lockout/Memory Parity Only
15 - 19	Memory or Controllers

The bus will support a maximum length of 55 slots or 33 active devices (40 inches).

INDEX

C.P. PACKAGE LOCATIONS

PAC		SLOT	PART No.
0AA01D		08	70050173-706
0AA02B		09	70050176-703
0AA03B		10	70050179-703
0AA04B		11	70050182-703
0AA05D		06	70050185-705
0AA06D		01	70050188-706
0AA07B		02	70050191-703
0AA08C		03	70050194-704
0AA09E		04	70050197-708
0AA10D		05	70050200-707
0AA11B		07	70050203-703
0BA74C	14	70032704-704	MEMORY OPTIONS.
0AA20B	12	70032122-702	DMC ADAPT.
0AB85A	06	60127045-701	RCP-701 ONLY.
0AA39C	MEMORY	70031634-707	4K -16 BIT.
0AA40C	"	70031634-708	4K -18 BIT.
0AB41A	"	60126093-702	8K -16 BIT.
0AB42A	"	60126093-701	8K -18 BIT.

REGISTERS

PROGRAMABLE	DISPLAY	NON-DISPLAY
A (Accumulator)	H (Halt)	I (D.M.A.)
B ('A' Reg. Extension)	M (Memory)	O (D.M.A.)
S (Address Pointer)	Y (Program)	F (Operation)
X (Index)		
P (Program)		
K (Status)		
J (Base Sector Relocation)		

MACHINE CYCLES

'F' Cycle - Instructions fetched from memory. 'F' and 'M' registers loaded.

'I' Cycle - Indirect address utilised.

X)
Y) Cycles - Data execution
Z) 'Y' is a non-memory cycle.

INTER-REGISTER INSTRUCTIONS

LDA '0	X Register
LDA '1	A Register
LDA '2	B Register
LDA '3	S Register
LDA '4	PUSH (Insert)
LDA '5	POP (Withdraw)

PUSH AND POP

PUSH

Push pre-decrements the 'S' register so that data is inserted under the last location.

i.e. 'S' = '100 next push ⟶ '77

POP

Pop post increments the 'S' register, so the data is poped, then the 'S' register is incremated.

SUMMARY OF KEY-IN LOADERS

Cartridge	Disk Moving Head	Fixed Head	Magnetic Tape 9- and 7-track	Cassette	ASR and High Speed Paper Tape	Cards
000013	000013	004014	010057	010057	010057	011057
0301dd	0303dd	010020	005005	073005	0300dd	000013
1716dd	005005	1714dd	101000	004017	1310dd	005005
003003	1715dd	000000	1714dd	1716dd	002003	1714dd
005017	177747	004007	000020	000017	101040	000020
1715dd	005010	1715dd	005010	1310dd	002003	005010
003006	1716dd	177620	1715dd	002006	010000	1715dd
0307dd	0u000h	000213	1777qq	141340	1310dd	177702
004002	004002	1716dd	005013	024000	002010	005013
1717dd	040240	000000	1716dd	1300dd	041470	1716dd
003012	0307dd	1312dd	tt1000	002012	1300dd	021011
1715dd	1717dd	0zz400	1315dd	110000	002013	1312dd
003014	003014	101110	003014	100040	110000	101000
100000	1715dd	002013	100040	002006	024000	101400
177747	003016	102020	003014	01400n	100040	003014

Defaults for Automatic Bootstrap Loading

DEVICE ADD → dd='45 dd='35 dd='22 9-track 7-track

UNIT NO. → u= 0 BOOTSTRAP SECTOR → zz='37 dd='14 dd='15 dd='21 dd=01 dd=05

HEAD NO → h= 0 OCTAL -UE WORD CNT FOR SECOND LEVEL LOADER qq= 02 qq='41 UNIT NO. → n= 0

TAPE DRIVE INDICATOR → tt= 02 tt= 02

VERIFICATION AND TEST PROGRAMS.

TESTED AREA	PROGRAM NAME
MAINFRAME INSTRUCTION TEST	AB16-CCT4
MEMORY TEST	A316-CMT5
POWER FAILURE TEST	AE16-PFT3
EXTENDED ADDRESSING TEST	AB16-05T3
MEMORY PARITY TEST	AE16-07T6
MEMORY LOCKOUT/BASE SECTOR RELOCATION TEST	AE16-08T4
HIGH SPEED ARITHMETIC TEST	AB16-11T1
REAL TIME CLOCK TEST	AB16-12T3
EXTENDED REAL TIME CLOCK TEST	AB16-TIME1
EXTERNAL REAL TIME CLOCK & WATCH DOG TIMER TEST	AA16-3000I1
64K MEMORY TEST	AA16-2022T1
64K MAINFRAME TEST	AA16-2022T2
DMA BUFFER BOARD TEST	AA16-9070I1
7-TRACK U-PAC MAG TAPE TEST	AE16-MTT2
7-TRACK U-PAC MAG TAPE BYTE MODE TEST (4020 ONLY)	AE16-4020I4
9-TRACK U-PAC MAG TAPE TEST	AE16-MTT3
DUAL CASSETTE TEST	AA16-5400I1
1600CPI MAG TAPE TEST	AB16-4180I1
1/9 TRACK SP-10 VLC MAG TAPE TEST (4041/4042/4051/4052/4053)	AA16-4051I1
AMC FIXED HEAD DISC TEST	AA16-4510I1
CDC MOVING HEAD DISC TEST 4620 & 4621	U16-46T3
UNIVERSAL MOVING HEAD DISC TEST (4700)	AB16-47T3
CARTRIDGE DISC TEST (4760)	AA16-4760I1
SP-10 MOVING HEAD DISK TEST	AA16-4780I1
PAPER TAPE READER & PUNCH TEST	AG16-RPT2
CARD READER - CARD READER/ PUNCH TEST	AB16-51XXT6
SP-10 CARD EQUIPMENT CONTROLLER TEST	AA16-51XXT5
5140 CARD READER/PUNCH TEST (PUNCH/FEED/READ TEST)	AB16-RPT4
ASR-33/35 TEST	AG16-TWT1
HISI U-PAC LINE PRINTER TEST	AB16-55T3"
SP-10 LINE PRINTER CONTROLLER TEST	AA16-55XXT4

SSLC TEST 8K (6312 & 6313)	AA16-6312T1
SSLC TEST 4K (6312 ONLY)	AA16-6312T3
DMA FOR SSLC TEST	AA16-6314T1
HDLC TEST	AA16-6315T1
LSMLC STATIC TEST (6321 ONLY)	AA16-6321T2
UMLC STATIC TEST (6322 ONLY)	A16-6322T2
MLC FUNCTIONAL TEST (6321 & 6322)	AA16-6322T1
MSLC TEST (6333 & 2605)	AA16-MLB9
CRC TEST (2050 & 2613)	AA16-CRC9
S2000 TO S700 COUPLER TEST (REFLECT MODE)	AA16-FEPR
S2000 TO S700 COUPLER TEST (CP TO CP TRANSFER)	AA16-FEPX
ANALOG TO DIGITAL TEST	016-ADT1
ANALOG INPUTS TEST	AA16-RTAIT1
ISOTHERMAL UNIT TEST	016-ITT1
ALARM PRINTER TEST	016-ATT1
3/5/716 DDC OAC TEST	AB16-RTDCT1
3/5/716 DIGITAL INTERFACE TEST	AB16-RTDIT2
Redundancy Switch	AA16-6930T9
SSLC TEST (316)	AB16-DC59
Terminal Control Unit	AA16-TCU9
716/316 ICCU (716)	AA16-3101T9
716/316 ICCU (316)	M16-3101T9
Floating Point Arithmetic	AA16-3111T9
716/716 ICCU	AA16-3100T9
HSDC TEST	AA16-HSDCT9
MSU0400	AA16-MSC9

TO LOAD PRE H716 TAPES

1. Put INA '10XX in 'A' register.
2. Put STA '3 in 'M' register.
3. Execute instruction in single instruct ('S' register loaded).
4. MASTER CLEAR.
5. Put OCP 00XX in 'B' register.
6. '1 to 'P' register.
7. Load tape.
8. Put machine to run and start.

SIGNAL NAME BREAK-DOWN

C M D R F W +

C - Core or Copy

H = Control panel.

I = Interrupt

B = I/O Bus

T = Timing

E = Emit (INTERNAL)

M = Memory

MD - From (Memory data bus)

RF - To (Register 'F')

W - Word

L - Low order bits

H - High order bits

- Polarity

SP-10 CIRCUIT BOARD NUMBERS.

NA ANN A

A → REVISION.

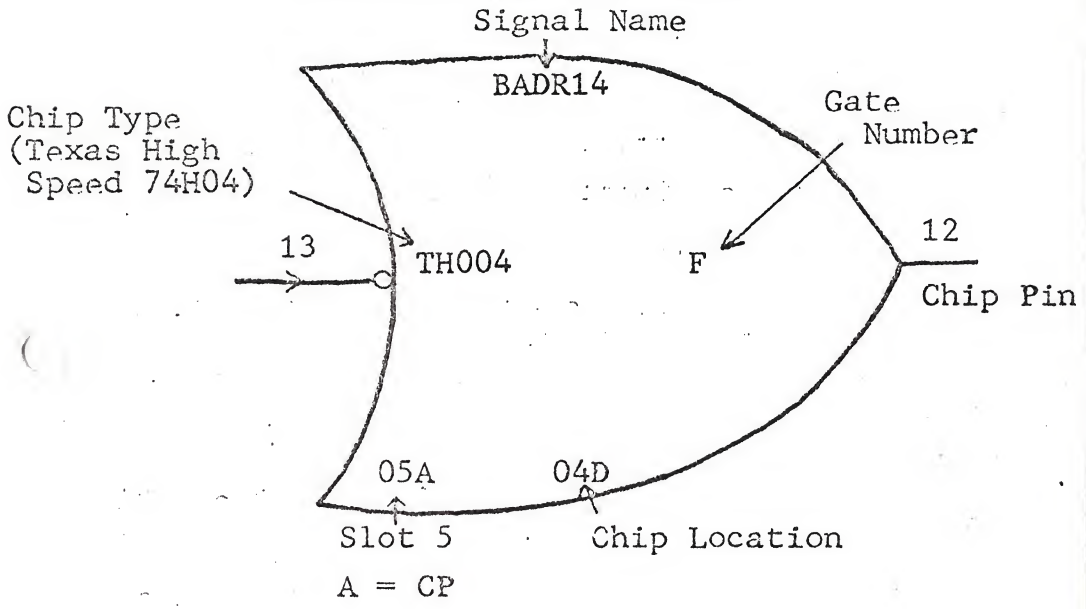
ANN → BOARD TYPE.

NA → INTERCHANGEABILITY INDICATOR.
ANY CHANGE REQUIRES AN EXTERNAL CHANGE.

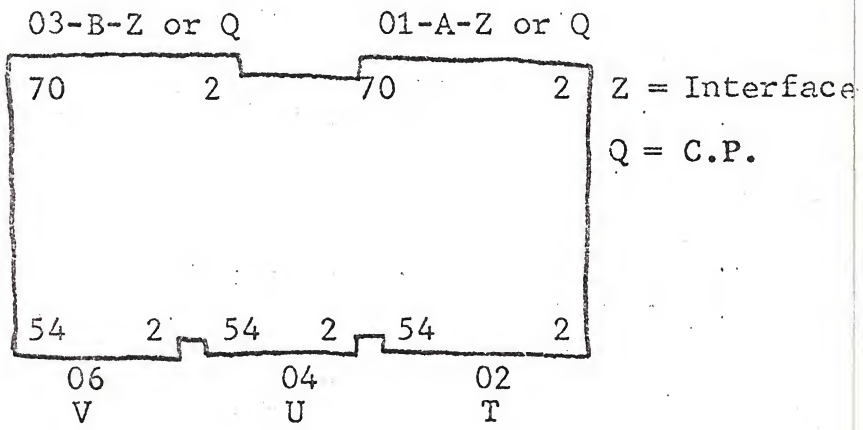
N = NUMERIC.

A = ALPHA.

CHIP SIGNAL DESIGNATION



SP10 TYPE CARD NOTATION



INTERRUPT PRIORITY

1. D.M.A.
2. D.M.C. (OPTN.)
3. Normal Interrupts ('63 + Device Address)
4. Standard Interrupts ('63)
5. Programmed I/O

Power fail and memory lockout violation override all others.

HARDWARE PRIORITY NETWORK

The higher the physical location of the option the higher the priority.

BINTPO - (PINA14) is the I/O interrupt line.

BDMAPO - (PINA5) is the DMA interrupt line.

Due to the backplane wiring and the circuitry on all option boards, when an option interrupts all low priorities are overridden and cannot interrupt until released by the higher priority.

EMPTY I/O BUS SLOTS

To ensure that the priority bus is continuous all empty slots must be wired as follows:-

Link Pins 5-6 (Except slots 13 and 14).
14-15 (Of the mainframe).

INTERRUPTS

PRIVILEGED ADDRESSES

'55 Watch Dog Timer
'56 Trace Mode
'57 Stack Overflow or Underflow
'60 Power Fail
'61 Real Time Clock
'62 Memory Lockout
'63 Compatible Mode

INTERRUPT OPERATION

The H716 has two modes of operation.
In compatible mode the interrupt is via '63.
In normal mode the interrupt is via '63 plus the device address.

i.e. For the teletype the address is '63 + 4 = '67

HARDWARE OPERATION

Force jump store to 'F' register.
Set M01
CMDRMW+
CMDRFW+
Change memory addressing gating.
Send BSTROB-
P + 1 → P
Inhibit further interrupts.

STANDARD DEVICE ADDRESS ASSIGNMENT.

00	Unassigned (Polling)
01	Paper Tape Reader
02	Paper Tape Punch
03	4th Line Printer WAS 1ST. L.P.
04	Teletype (1st)
05	Card Reader
06	Card Punch
07	Teletype (2nd) WAS FIXED HEAD DISC.
10	Unassigned (DMC Mag Tape)
11	Unassigned (DMC Mag Tape)
12	Unassigned (DMC Mag Tape)
13	Unassigned (DMC Mag Tape)
14	1st 9-Track Mag Tape
15	1st 7-Track Mag Tape
16	2nd 9-Track Mag Tape
17	2nd 9-Track Mag Tape
20	516 SMK
21	Cassette
22	Fixed Head Disc
23	RTI-B
24	516 SMK
25	2nd Moving Head Disc
26	2nd Card Reader/Punch WAS STORAGE DISPLAY.
27	RTC/WDT
30	RTI-A
31	1st HDLC or 8th SSLC } PARALLEL I/O CHANNEL.
32	2nd HDLC or 7th SSLC }
33	3rd HDLC or 6th SSLC or Floating Point
34	4th HDLC or 5th SSLC SKS/OCP OPTION.
35	1st Moving Head Disc or DN2000/PSI
36	2nd Line Printer or ICCU
37	1st Line Printer or 360 Coupler
40	2nd Cartridge Disc

41	Unassigned	R.T.I 'A'
42	Unassigned	
43	Unassigned	
44	Unassigned	
45	1st Cartridge Disc	
46	2nd UMLC or HSDC (Hemel Display)	
47	2nd UMLC or 3rd Line Printer	
50	3rd UMLC SOFTWARE MULTILINE CONTROLLER.	
51	1st MSLC or 3rd UMLC	
52	2nd MSLC	
53	3rd MSLC	
54	4th MSLC or 2nd LSMLC	
55	1st LSMLC	
56	1st UMLC (requires 2 continuous addresses)	
57	1st UMLC	
60	1st SSLC or 8th HDLC	
61	2nd SSLC or 7th HDLC	
62	3rd SSLC or 6th HDLC	
63	4th SSLC or 5th HDLC	
64	CRC	
65	Unassigned	
66	4th UMLC or 1st BM-UMLC	
67	4th UMLC or 1st BM-UMLC	
70	4th Autocall or Redundancy Switch	
71	1st Autocall	
72	2nd Autocall	
73	3rd Autocall	
74	Document Handler (Hemel)	
75	TV Monitor, Alphanumeric Display (Hemel)	
76	TV Monitor, Graphic Display (Hemel)	
77	I/O Bus Tester	

DEVICE IDENTIFICATION ASSIGNMENTS

When a device is polled via an INA '11XX instruction, it will reply with its I.D. Code.

00X	Unassigned	27X	Shared Memory Optn.
01X	PTR	30X	Low-Cost Line Printer
02X	PTP	31X	Low-Cost Card Reader.
03X	H112 Line Printer	32X Thru 0777X)	Unassigned
04X	Teletype		
05X	System Interface	1000X	I/O Bus Tester
06X	9 Track Mag. Tape		
07X	Fixed Head Disc		
10X	Real Time Clock		
11X	Cassette Tape		
12X	Moving Head Disc		
13X	Data Line Cont.		
14X	Computer Couplers		
15X	Interrupts		
16X	R.T.I. 'A'		
17X	Message Mode Adapt.		
20X	L.S.M.L.C.		
21X	U.M.L.C.		
22X	A.S.L.C.		
23X	S.S.L.C.		
24X	R.T.I. 'B'		
25X	Software Multi Cont.		
26X	Multi-Line Buffer		

COMPATIBLE MODE INTERRUPT MASK ASSIGNMENTS

DATA BIT (BDATXX-)	DEVICE
01	Mag. Tape Control Unit 1
02	Mag. Tape Control Unit 2
03	Unassigned
04	Moving Head Disc
05	I/O Channel 1
06	I/O Channel 2
07	I/O Channel 3
08	Small Mass Store
09	P.T.R.
10	P.T.P.
11	ASR - 33/35
12	Card Reader
13	Unassigned
14	Line Printer
15	Unassigned
16	R.T.C.

MAINTENANCE SWITCHES

SINGLE CYCLE - Allows the processor to execute one cycle for each operation of the start switch.

MEMORY CYCLE - Allows continuous access to memory after depression of start switch. This may be either FETCH or STORE in a single address (P) or consecutive addresses (P+1).

CAUTION

A consecutive store (P+1) will over write the Key in loader.

R.O.M. Used with R.O.M. memories only.

H716 I/O BUS SIGNALS

PIN	SIGNAL	DESCRIPTION
	BDAT01 Thru 16	Data Bits 1 - 16
	BADR01 Thru 16	Address Bits 1 - 16
A67	BDRLIN -	Device Ready Line
A68	BSTROB -	Strobe
A60	BPRGIO -	Programmed I/O
A59	BPWRFL -	Power Fail
A69	EMSTCL -	Master Clear
B11	BINTRQ -	Interrupt Request
A62	BDMARQ -	D.M.A. Request

MAINFRAME POWER DISTRIBUTION

SLOT	LEFT HAND SCREWS	RIGHT HAND SCREWS
1	-5	+22
2	-12	+15
3	GND	GND
4	GND	BPWRFL-
5	+12	+5 BAT*
6	+5A	HMSTCL-
7	-5	+22
8	-12	+15
9	GND	GND
10	GND	BPWRFL-
11	+12	+5 BAT*
12	+5B	HMSTCL-
13	-5	+22
14	-12	+15
15	GND	GND
16	GND	BPWRFL-
17	+12	+5 BAT*
18	+5C	HMSTCL-
19	Not Used	Not Used

* This point is connected to +5 volts on the OAA05X mainframe board.

NOTE:
BPWRFL- IS BULK POWER FAIL.

COMMUNICATIONS POWER DISTRIBUTION

SLOT	LEFT HAND SCREWS	RIGHT HAND SCREWS
1	-	-
2	-12	-
3	GND	GND
4	GND	BPWRFL-
5	+12	-
6	+5A	HMSTCL-
7	-	-
8	-12	-
9	GND	GND
10	GND	BPWRFL-
11	+12	-
12	+5B	HMSTCL-
13	-	-
14	-12	-
15	GND	GND
16	GND	BPWRFL-
17	+12	-
18	+5C	HMSTCL-
19	Not Used	Not Used

NOTE
BPWRFL- IS BULK POWER FAIL

MEMORY VOLTAGE MARGINS

N.B. On no account should the modules be tested beyond the specified ranges.

D.C. VOLTAGE	LIMIT	0°C	20°C	60°C
+15	MIN	15.0	14.0	13.0
+15	MAX	17.0	16.0	14.4
+22	MIN	22.0	20.5	19.0
+22	MAX	25.0	23.5	21.0

POWER SUPPLY PART NUMBERS. 5Hz.

POWER SUPPLY.	OLD.	COST REDUCED.
C.P.U.	70031955-~~708~~712	60125653-~~704~~718
~~OPTN.~~	~~"-708~~	"-706
COMMS	"-~~709~~713	"-~~705~~720

~~60123350-720~~

REGULATORS.	OLD.	BOARD TYPE.	COST REDUCED.	BOARD TYPE
+5v	70031114-703	(OAA 43A)	60125942-701	(OAB 38A)
-5 ±12v	70031314-705	(OAA 45A)	60127527-701	(OAA 45B)
+15v	70031187-702	(OAA 44A)	70031187-702	(OAA 44A)
+22v.	70031416-707	(OAA 47B)	70031416-707	(OAA 47B)
-12v.	70031314-704	(OAA 46A)	70031314-704	(OAA 46A)
+12v.	70031416-708	(OAA 48B)	70031416-708	(OAA 48B)

BULK W/MAJOR BOARD.	OLD.	COST REDUCED.
	70031714-702	60125651-702

TRANSITION BOARD.	OLD.	COST REDUCED
CPU	NONE	60125936-701
OPTN.	NONE	60125936-702

MEMORY ADDITIONS

NOTE: Empty I/O Bus slot priority jumpers A05 to A06 and A14 to A15 must be deleted as required.

[redacted] Memory Modules

Memory enable jumpers must be installed from Pin B53 of the 4K module or the first 4K of an 8K module and Pin B16 of the second 4K of an 8K module under installation to the following mainframe pins.

MODULE	SIGNAL SOURCE
MENBL0-	06A41
MENBL1-	06A43
MENBL2-	06A39
MENBL3-	06A37
MENBL4-	06A32
MENBL5-	06A55
MENBL6-	06A53
MENBL7-	06A51
MENBL8-	06A49
MENBL9-	06A56
MENBLA-	06A54
MENBLB-	06A52
MENBLC-	06A50
MENBLD-	06A44
MENBLE-	06A46
MENBLF-	06A48

Expansion above 32K is an option and is covered with 8K memory modules on Page [redacted]. NEXT

Bus Jumpers.

MEM+I/O Draw to Draw.

	FLEXI
A01 - A34	60133773-001
A37 - A70	-002
B01 - B34	-003
B37 - B70	-004

I/O Draw to Draw.

	FLEXI
A01 - A34	60133773-005
A37 - A70	-006
B01 - B34	-007
B37 - B70	-008

MEM + I/O Backplane to Backplane.

	FLEXI	P.C. Board.
A01 - A34	60133773-001	70050124-701
A37 - A70	-002	70050130-701
B01 - B34	-003	70050133-701
B37 - B70	-004	70050136-701

I/O Backplane to Backplane

	FLEXI	
A01 - A34	60133773-005	70050139-701
A37 - A70	-006	70050142-701
B01 - B34	-007	70050145-701
B37 - B70	-008	70050148-701

EXTENDED MEMORY ENABLE JUMPERS

These jumpers must be installed from the OAB15A interface board in slot 01 of the memory expansion bus, to pin B53 of the 4K module or the first 4K of an 8K module and pin B16 for the second 4K of an 8K module.

OAB15A 70033152-701

20K	MENBL4-	01A01
24K	MENBL5-	01A34
28K	MENBL6-	01A40
32K	MENBL7-	01A54
36K	MENBL8-	01A55
40K	MENBL9-	01A64
44K	MENBLA-	01B07
48K	MENBLB-	01B08
52K	MENBLC-	01B16
56K	MENBLD-	01B34
60K	MENBLE-	01B53
64K	MENBLF-	01B57

8K Memory Modules

For the first 4K the enable jumper should be connected to pin B53 and for the second 4K to pin B16..

Extended Memory

Expansion above 32K requires a memory option bus with an OAB15A in slot 1, in the case of 4K modules. Using 8K modules only the memory option board in CP slot 14 need be used, up to 64K without the bus.

NOTE:

The board in CP slot 6 must revision D or later to support 8K modules.

Configuration Wires for the Extended Memory Bus

Add 01B35 - 01B49 ZV+05BAT
Add 01B36 - 01B50 ZV+05BAT

Add CP14A02 - 01A02 MPROPT+
Add CP14A04 - 01A04
Add CP14A06 - 01A06

MEMORY OPTION JUMPERS

CAA74A Memory parity only
OBA74A Parity, lockout and extended addressing

When one of the above packages are installed in slot 14 the following jumpers must be installed.

To enable Memory Parity

Delete 14A64 - 14A70 MPARER+
Delete 14A02 - 14A09 MPROPT+ (if OBA74A)
(To test ground 14B67)

To enable Memory Lockout

Delete 14B08 - 14B23 MLOOPT+A
Delete 05B20 - 05B23 MLOOPT+
Add 01B24 - 05A19

To enable Extended Memory (32K to 64K)

Delete 14A07 - 14A23 M64K01+
Delete 14A34 - 14A40 MCIREQ-X
Delete 14A47 - 14A59 M64K02+
Delete 14A55 - 14A63 MADD02-
Delete 14B47 - 14B66 M64OPT+

Add 14A40 - 14A53 M64KCT-A
Add 14A63 - 14A70 M64K02-A (14A67)
Add 14B03 - 15A59 BPWRFL-A
Add 06B24 - 14A13 RKEAMD+H
Add 11B40 - 14A11 ERXAUW+
Add 06B62 - 14A15 ERYMAW+

MAINFRAME OPTION JUMPERS

To enable High Speed Arithmetic

Delete 01B47 - 01B50 HSAOPT+

To enable Base Sector Relocation

Add 05A19 - 01B24 BSROPT+

I/O BUS TERMINATION

A terminator is provided on the last slot to prevent ringing on the function BSTROB.

This circuit module plugs onto backplane pins A36 through A70.

NOTE:

DO NOT INSTALL OPTIONS

WITHOUT AUTHORISATION

KNOWN PROBLEMS

FAULT	RECTIFICATION
1. Early RTC/WDT address changed due to clash with another option.	Was 10_8 is 27_8 no effect.
2. RTC a.c. input terminal rivets break away from the solder and become intermittant.	Solder wire through hole in rivet to tag and track.
3. Power supplies unstable +5 volt regulator at power on. (OAA43A)..	Change R10 from 20 ohms to 200 ohms.
4. S.S.L.C. 'Current Mode' is not compatible with U35 modems.	None.

5. SLOT 18 PIN 5 TO SLOT 19 PIN 6 DMA PRIORITY NETWORK ETCH MAY BE MISSING ON THE MAIN FRAME.

6. EXTENDED MEMORY OPTION -2022 MAY CAUSE PFI INTERRUPTS CAUSING PROG. TO HANG IN UPPER CORE. ADD PULL UP TO BP WRFL-W ON OAA15A BOARD. DIP SITE 32B PIN 09 TO CONNECTOR A PIN 59.

DMA SIGNAL SEQUENCE (LDB 135)

1	TPULSE+7	(H)		
	TPULSE--Y	(L)		
	IATRRQ-	(H)	A4	
	IFDARQ		B4	DMA Request
2	TPULSE+7	(L)	E4	
	OFRREK		E2	
	IA/IBK-E	(H)	G6	
	MCIREQ-	(H)	150A2	Prevents MEMCIN+ 188 G11
	IARQFN+	(L)	F4	Inhibits BRQENB-
3	IASH01		137B1	IASH10, 137E1 fired.
4	EJXMAW+		129D4	and EMFMAW+ 129D1 inhibited.
	EBAMAW+		129C1	enabled. Address formed by BADR lines.
5	IFMECI	(H)	136E10	Set
	MCEREQ-	(L)	150A1	Low
	MHDSHK		150E10	Acknowledges cycle request.
	IADATA-		135G10	Inhibits MCIMLF 150C8 & MCINRT 150C10.
	IASH02		137E7	Fired.
	IASH04		137B5	Fired. Guarantees BSTRO width
	IASH02		Time Out	
	IASH03		137G8	Fired by IASH02 time out.
	IARQEN		135F4	Re-enables DMA request.
	BCLPRN		138F10	
	IFMECI		136E10	Cleared
6	IADRDY-		137C6	Generated (DMA data ready)
	IASH05			Clears IFSTRB on time out.
	IASH06			Gives EROBDW+ 136G11.
7	IARQEN+		135F4	Re-starts IASH01 chain for further cycles.

ONE SHOTS

OPTION 5565 222 LINEPRINTER

The following one shots can be checked whilst doing a print and space operation.

PACSS+	01A28B13	45-53 ms
HMDLY+	01A32B05	17-23 ms
SBYDL+	01A32B13	5-9 ms

These one shots are not adjustable so if outside specification the dip (T123) must be replaced.

WATCH DOG TIMER

Signal WATCH + should be 1150 to 1350 ms wide.

If necessary R4 (20K on standoffs) may be altered within small margins to obtain the desired pulse width.

ASR/KSR

Monitor CLOCI+ (01A14E03) whilst holding down repeat and any character. Adjust POT1 (01A16G) so that the pulses are 9.1 ms apart.

Monitor CLOCO+ (01A18F13) whilst running a simple O/P loop program adjust POT2 (01A18G) so that the pulses are 9.1 ms apart.

Monitor CODLY- (01A20F13) and adjust POT3 (01A20G) to give an 18.2 ms pulse.

POWER SUPPLIES

BULK POWER SUPPLY VOLTAGES

DC Volt	O/P Load	Spec Volts at Test Load. Min	Norm	Max	Test Load	Max Increase at Reduced Load. Min Load	Max Load
+24	11.5A	23.2	24	25.2	9.5	1.0A	28.5
-24	0.3A	-24	-26.4	-27.7	0.3A	0.03A	-28.5
[illegible]	0.9A	19.4	20	20.6	0.9A	0.09A	23.0
+60	2.9A	58.2	60	61.8	2.5A	0.2A	70.0

REGULATED POWER SUPPLY VOLTAGES

DC OUTPUT	REGULATION	OVER VOLTAGE TRIP POINT	CURRENT MAX.	CURRENT MIN.
+5	±5%	+6.3	30.0	0
-5	±5%	-6.3	2.2	0
+12	±5%	+15.00	0.5	0
-12	±5%	-15.00	0.25	0
+24	⏥ 20 to 27 volts	-	0.72	-
[illegible]22	±5%	+28.00	1.0	0
+15	±5%	+18.00	6.5	0.2

Maximum total power output at any one time 265 watts.

OPTION 2050/2613

DESCRIPTION.

The Cyclic Redundancy Check option (CRC) allows a single option to perform CRC operations on data used with several different devices. It consists of two boards connected by a top-hat connector.

0AB05A	41264260-001
0AB06A	41264264-001

OPTION 2600

DESCRIPTION.

DATA NET COUPLER consists of two boards which require the standard I/O Bus.

0AB07C	42505917-002
0AB08A	42505918-001

OPTION. 3000

DESCRIPTION.

Real Time Clock and Watch Dog Timer consists of two independant clocks, one line and one crystal interrupting at 10μS to 40.96ms., and a wathdog timer which interrupts if not reset every second or sooner.

OAA12B 70050216-703

OPTION 716

Description

The basic processor occupies 10.5" of vertical rack.

Wires

Attach the Real Time Clock signal wire (red) to 05A02248 (LEFT HAND TERMINAL) and the ground wire to 05A02238 (RIGHT HAND TERMINAL).

ADD PAGES.

OPTION 3010

Description

Data Multiplex Control

This option is a single ~~wire wrap~~ board, ~~but because of its thickness it uses two slots in the I/O bus, the first being~~ in slot 12. In addition to this there is a 1 x 3 u bloc located in the first u pac option draw.

POWER FAIL DETECTION OF THE μPAC POWER SUPPLIES IS PROVIDED. ADJUSTMENT IS PROVIDED BY MEANS OF A POTENTIOMETER.

OPTION 3030.

DESCRIPTION.

BSC Down-line Load option uses a 2K ROM to load from the host system via an S.S.L.C. The R.O.M. must be configured as the next memory after the first 4K. and requires as pre-requisites 710-3000 (RTC+WDT.) plus the SSLC.

OAA69B 70032560-704

OPTION. 3100

DESCRIPTION.

Inter-communication unit (ICCU) for use between two Series 700 machines using DMA.

OAC24A 60127042-701

+5V. 3AMPS.
-5V. 500MAMPS.

U&T AM16-3100T9.

OPTION. 4041/4051

DESCRIPTION.

7/9 Track U.L.C. Magnetic Tape operating at 26ips will recording densites of 200, 556 & 800 Bpi in the case of 7 track and 800 bpi only on 9 track. The controller consists of a DMA Buffer board and a six slot back plane fitted with two control boards.

ODA82C	70032912-706.	BOARD #1
ODA83C	70032913-706	BOARD #2
OBA81A	70032862-710	BACKPLANE
OAA22B	70031557-702	DMABB.

WARNING.

The boards on this option are now on their third non-interchangeable level.

SEE TSB 710.01-025 REV 02. PAGE 8.

OPTION. 4053

DESCRIPTION.

CRC OPTION FOR 4051 MAG. TAPE.

OAB16A	70033061-701	BOARD 5
OBB16A	70033061-702	

OPTION 41XX/402x

Description

Magnetic Tape 9track and 7track. (and 4x3 µ pac)

The option is a 6 x 3 u pac unit which requires a 716 - 3010 D.M.C. to make it 716 compatible.

OPTIONS 4510, 4511, 4512 and 4513

Description

Fixed Head Disc. 64K, 128K, 256K and 512K

This is an I/O option consisting of:-

1. An ~~wire wrap~~ OAA22B board (DMABB) requiring ~~two slots in~~ the I/O bus. Address '22 must be configured.

2. Two interconnecting cables to connect the DMABB to the controller.

3. A controller consisting of a 6 pac prewired backplane and two ~~wire wrapped~~ controller boards.

4. One device cable a maximum of 11ft long.

5. Up to 4 disc drive assemblies.

Size

The device requires 10.5" of vertical rack and must be placed 3.5" from the bottom of the cabinet. If an air plenum is used in the cabinet then it must be 7" from the bottom.

OAA37B	70031554-702	BOARD 1
OAA38B	70031555-702	- 3
OAA73A	70032298-703	BACKPLANE. WINCHESTER CONNECTOR
OAA22B	70031557-702	DMABB
OAA73A	70032298-704	BACKPLANE. VIKING CONNECTOR.

OPTION 45XX Cont.

Configuration

The DMABB address must be configured on the dip in location 01A40B to be identical to the associated controller (LBD7700 B8). A logic one is available when the jumper is removed.

B = Standard interrupt.

1 = Address 1

2 = Address 2

3 = Address 3

etc.

OPTION 4514

Description

Additional 512K word fixed head disc.
Up to three 4514's may be added.

Size

Each device requires 10.5" vertical rack and must be configured directly above other 4500 devices.

Configuration Wires (LBD 6917)

1. (a) When first 4514 is added to 451X,
Delete 03A08E02 to 03A06E09
Add 03A08E06 to 03A06E09

(b) When second 4514 is added,
Delete 03A08E03 to 03A06E11
Add 03A08E07 to 03A06E11

(c) When third 4514 is added,
Delete 03A08E04 to 03A08E13
Add 03A08E08 to 03A08E13

2. Memory select and disc ready must be configured for numbers 2, 3 and 4 at XXX07 and XXX08 respectively on the additional devices.

OPTION 4760.

DESCRIPTION.

Cartridge disc controller

OAC02C	60126004-703
OAA22B	70031557-702

OPTION. 4780/4/81/4790

DESCRIPTION.

Moving head disc.

OAB67B	60123889-702	BOARD 1
OAB68B	60123890-702	BOARD 3.
OAB69A	60123891-701	BOARD 5
OAB84A	60123892-701	BACKPLANE
OAA22B	70031557-702	DMABB.

OPTION 5010

Description OAA14B 70050218-704.

300 c/s paper tape reader and control unit.

The controller requires a single I/O bus slot.

OPTION 52XX

Description

Paper tape punches.

5250 Low speed punch requires 14" vertical rack.
5260 High speed punch requires 14" vertical rack plus 3.5" for the electronic unit.

Wiring

The connector to the control unit is on 02Z.

OAA13C	70050217-704.	
OAA42A	70050152-701	+5 VOLT REGULATOR.
OAA52A	70050020-701	SOLENOID DRIVER.

OPTION. 5151/52/56/57

DESCRIPTION.

OUP CARD READER.

OAC27B	60124959-713	CONFIGURABLE.
OAB80A	60126358-701	SUPERCEEDED BY OAC27B.
OBB80B	60126358-707	" " "

OPTION. 5161/2/3/4, 5172/6

DESCRIPTION.

Card reader controller.

OAC28B	60124959-712.	CONFIGURABLE.
OAB65B	60124954-702	PUNCH DEVICES ONLY
OBB98B	60126387-708	SUPERCEEDED BY OAC28B.
OBB64B	60126387-707	" " "
OBB79B	60126388-707	" " "
OBB99B	60126388-708	" " "

OPTION 5210

DESCRIPTION.

Teletype BRPE-11 paper tape punch and controller.

OAA13C	70050217-704	
OAA42A	70050152-701	+5V REGULATOR.
OAA52A	70050020-701	SOLENOID DRIVER.

OPTION 5300

DESCRIPTION.

ASR/KSR 33/35 Teletypewriter

OAB11B	70050536-703	
OAA21B	70032166-702.	{ NO EIA DRIVER BUT GETS OUT OF TROUBLE.

OPTION 5400

Description OAA79A 70032719-702

Cassette tape and one drive which operates on PIO.

It consists of:

(a) One ~~wire wrap~~ control board requiring ~~two slots on~~ the Qbus. Address '21 must be configured.

(b) One cassette rack mounting assembly housing one 5400 or two 5400 and 5401 cassette handlers and a power supply.

OPTION 5541/2 AND 5551/2.

DESCRIPTION.

Serial and OUP Line printer.

OAC03A 60125819-701

OPTN 6312, 6313, 6314.

DESCRIPTION.

6312 SYNCHRONOUS SINGLE LINE CONTROLLER. (SSLC.)
6313 CODE CONVENTION OPTION. (CCO)
6314. DIRECT MEMORY ACCESS OPTION. (DMA.)

NEW	DMA	6314	70032930-701	OAA84A.
NEW	SSLC	6312	70032964-701/5	OAB09A
NEW	CCO	6313	70032971-701	OAB10A
OLD	SSLC	6312	70032095-702	OBA17A *
OLD	CCO	6313	70032097-702	OBA18A *

* NOT TO BE USED WITH 6314 DMA OPTION.

OPTION. 5565/6/7/8/9, 5576/5577

DESCRIPTION.

LINE PRINTERS 112/222A/112N

OBB66B	60123942-704	
OAA22B	70031557-702	DMA BB.
OAB66A	60123942-701	{ EARLY TYPE DIFFERENT DEVICE CABLE.

OPTION 6315

DESCRIPTION.

HDLC SYNCHRONOUS SINGLE LINE CONTROLLER.

OAC30A	60125867-701	DMA ADAPT.
OAC31A	60126129-701	BOARD 01
OAC32A	60125861-701	BOARD 03
OAC33A	60125862-701	BOARD 05
OAC34A	60127298-701	BACKPLANE.

OPTION. 6316

DESCRIPTION.

MIL STANDARD 188C

OBA80B	70050493-703

OPTION 6321

Description

Low Speed Multiline Controller.

The option requires two slots in the I/O bus plus 12 adjacent slots in a non I/O bus expansion backplane. (6 boards in 12 slots).

Also required are line module adaptors (MAX.4) each capable of driving 32 lines via line modules in a 6 slot backplane. (Max. No. lines 128)

Slot and Board No.	Type	
1	0AA31A	70032300-701
3	0AA32A	70032303-701
5	0AA33A	70032304-701
7	0AA34A	70032305-701
9	0AA35A	70032306-701
11	0AA36A	70032307-701
DMABB	0AA30A	70032312-701
BACKPLANE	0AA71A	70032385-702
LINE MODULE ADAPTER.	0AA52A	70050213-701

Cables

Lines	Line Module Adaptor Zone	LSMLC Zone	LSMLC Board
6341A 0 - 31	02Z	02Z	11
	04Z	02Z	09
6341B 31- 63	02Z	04Z	11
	04Z	04Z	09
6341C 64- 95	02Z	02Z	07
	04Z	02Z	05
6341D 96-127	02Z	04Z	07
	04Z	04Z	05

OPTION 6321 Cont

Bus Adaptor Cables

DMA Adaptor Card Zone	Option Board	Option Zone
02Z	03	02Z
04Z	03	04Z

Logic and Configuration

Zone	Board	
06Z	01	INTERCONNECT TO ZONE 06Z BOARD 03
04Z	01	Configuration. Baud rates of line modules.
06Z	05	Configuration. Baud rate 1, character length.
06Z	07	Configuration. Baud rates 4, 5 and 6
06Z	09	Configuration. Baud rate 3 + parity.
06Z	11	Configuration. Baud rate 2 + No. stop bits.

OPTION 6350.

DESCRIPTION.

RELAY INTERFACE.

0AB74A 70050539-701

OPTION 6322

55 SYNC.
56 ASYNC.

Description

Universal Multi-line Controller.

The option consists of:

(a) One DMA adaptor requiring ~~two~~ 1/O ~~slots~~.
ONE 0AC39A 60126909-701 FOR BLOCK MODE OR
0AA30A 70032312-701

(b) One UMLC 12 slot backplane (70032424-701).0AA85A

(c) Five ~~wire wrap~~ logic boards.

Also a maximum of 4 line module adaptor units and up to 32 line modules. Maximum No. lines 64.

Slot	Board	
01	0AA25B	70032302-702.
03	0AA26C	70032308-703
05	0BA27A	70032309-703
07	0BA28A	70032310-703
09	0BA29A	70032311-704
LINE MODULE ADAPTER	0AA52A	70050213-701

Cables

Lines		LMA Zone	U.M.L.C. Zone	U.M.L.C. Board
6341A	0 - 15	02Z	02Z	07
		04Z	02Z	03
6341B	16 - 31	02Z	04Z	07
		04Z	04Z	03
6341C	32 - 47	02Z	02Z	09
		04Z	02Z	05
6341D	47 - 63	02Z	04Z	09
		04Z	04Z	05

DMA Adaptor	U.M.L.C. Zone	U.M.L.C. Board
02Z	02Z	01
04Z	04Z	01

OPTION 6351/52/53.

DESCRIPTION.

LINE MODULES.

OAA51B	70050225-702	ASYNC. ~~2400~~ 300
OAA56A	70050249-701	ASYNC. 2400.
OAA55A	70050253-701	SYNC. 10·8K.

OPTION 6333

Description

Multi-Line Controller. OR MSLC OR MLB.

The option consists of:

(a) One interface board OAB01A. 41264112-001

(b) One or two 6 pac backplanes.

(c) One MLB bus adaptor board. OAB02C. 41264129-002

(d) One to eight line buffer boards in any mixture of sync. and assync.

OAB03C Sync. Line module. 41264143-002
OAB04C Assync. Line module. 41264145-002

Cables

I/O ~~DMA~~ Adaptor	Bus Adaptor	
02Z	02Z	
04Z	04Z	
	06Z	Address Configuration*

* For standard address of '51 the connections are:

5 to 6, 13 to 14 and 17 to 18.

OPTION 6365/2622.

DESCRIPTION.

AUTO DIAL FOR 6333

OAB14A 41202618-001

OPTION. 6901/6902.

DESCRIPTION.

AUTO CALL

OAA77A 70032710-701

OAA78A 70032710-702

OPTION 9040

Description

u Pac draw with power supply. PB 333A.

Power supply occupies 2 x 3 area leaving 4 x 3 and 6 x 3 areas free for standard u pac use.

Size.

Uses 7" of vertical rack.

Wiring

Use B70033088-701 power distribution kit when connector plane is adjacent to the power supply and B70033088-702 kit in the larger area.

~~OPTION 905X~~

~~Power supplies.~~

OAA54C 70050328-703 REGULATOR.

OPTION. 9050

DESCRIPTION.

716 POWER SUPPLY.

OAA43B	70031114-703	+5
OAB38A	60125942-701	COST RED. +5
OAA44B	60127530-701	+15
OAA45A	70031314-705	-5 ±12v.
OAA45C	60127527-702	COST REDUCED. -5 ±12v.
OAB39B	60127870-701	TRANSITION BRD. (CPU.)
OAB47B	60127870-702	TRANSITION BOARD (OPTNS)
OAA46A	70031314-706	-22v.
OAA47B	70031416-707	+22v.
OAA48B	70031416-708	+12v.
OAA49B	70050379-702	CAPACITOR BOARD.

OPTION. 9070.

DESCRIPTION.

DMA BUFFER BOARD.

OAA22B 70031557-703.